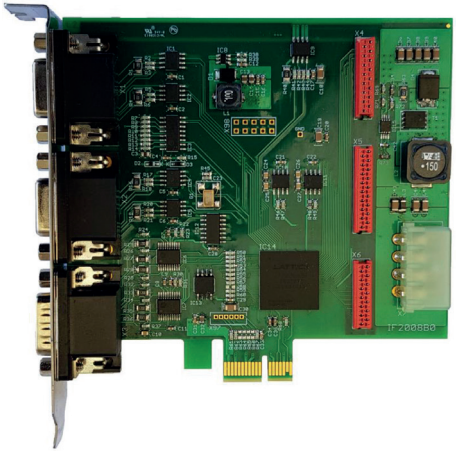
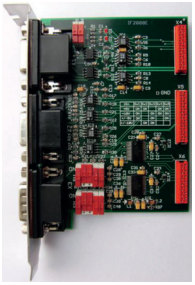
MICRO-EPSILON





Assembly Instructions

IF2008/PCIe, IF2008E

Interface board

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Contents

1. Safety

Board operation assumes knowledge of the assembly instructions.

1.1 Symbols Used

The following symbols are used in these assembly instructions:

NOTICE	Indicates a situation that may result in property damage if not avoided.
➡	Indicates a user action.
i	Indicates a tip for users.

1.2 Warnings

NOTICE

Electronic devices can be damaged due to electrostatic discharge. Prior to installation of the interface card(s), we recommend to touch a grounded surface in order to avoid electrostatic discharge. For that purpose please touch a grounded surface, for example the metal housing of your computer.
> Damage to or destruction of the board.

1.3 Proper Environment

- Temperature range
  - Operation: 5 ... +40 °C (41 ... +104 °F)
  - Storage: -10 ... +40 °C (+50 ... +104 °F)
- Humidity: 5 - 95 % (no condensation)
- Pressure: Atmospheric pressure

2. Delivery

- 1 IF2008/PCIe and/or IF2008E interface board
- 1 CD-ROM with software package, driver for windows ®10
- 1 Assembly instructions
- 1 Adapter for power supply

➡ Check for completeness and shipping damage immediately after unpacking.

➡ In case of damage or missing parts, please contact the manufacturer or supplier.

3. System Requirements

- Processor (CPU) with 1 GHz clock rate or faster
- 2 GB RAM
- Windows ® 7 (32/64 Bit), Windows ® 10 (32/64 Bit)
- Free PCIe slot
- Minimum 10 MB free disk space on the hard disk

4. Technical Data

4.1 IF2008/PCIe Basis Board

Mechanics and environment

- Dimensions (PCB) approx. 110 x 105 mm, width: 1 slot
- Max. permitted ambient temperature +40 °C (+104 °F)
- 2x D-SUB female connectors HD 15-pin for sensor connections
- 1x D-SUB male connector HD 15-pin for encoder signals
- 1x Tyco/AMP Commercial MATE-N-LOK connector (IDE hard drive connector) for supply DC/DC-converter,
- 3x Tyco/AMP MicroMatch female connectors to IF2008E

PCI-Express bus

- PCI-Express x1 interface
- Target Interface (slave) according to specification Rev. 1.0
- Current consumption at +3,3 V approx. 0.5 A, without sensors and encoders
- Power supply of encoders with +5 V from the PCI power
- Power supply of the sensors with +24 V from the PC power supply

Sensor interface (X1 / X2)

- 4x RS422 drivers (2x TxD and 2x trigger out) and 2x RS422 receivers per connector (input/output frequency max. 5 MHz)
- Power supply of the sensors 24 V

Encoder interface (X3)

- Interface for two encoders with 1 Vss, RS422 (difference) or TTL (single-ended) signals
- Power supply of the encoders with +5 V from PCI power supply without galvanic isolation (current consumption dependent on the connected encoders)
- Interpolation programmable from 1 to 64 times for encoders with 1 Vss signals
  (input frequency max. = [3.2 MHz / interpolation] ≤ 800 kHz)
- Evaluation programmable from 1 to 4 times in case of encoders with:
  - RS422- / Difference signals
    (input frequency max. 800 kHz)
  - TTL- / single-ended-signals
    (input frequency max. 400 kHz)

4.2 IF2008E Expansion Board

Mechanics and environment

- Dimensions (PCB) approx. 71 x 102 mm, width: 1 slot
- Max. permitted ambient temperature +40 °C (+104 °F)
- 1x D-SUB female connector HD 15-pin for sensor connections
- 1x D-SUB female connector 9-pin for IO interface
- 1x D-SUB male connector 9-pin for analog inputs
- 3x MicroMatch female connectors for connection to IF2008/PCIe

Sensor interface (X1)
- Identical to IF2008/PCIe (X1)

I/O-Interface (X2)
- 4x Optocoupler inputs, input current max. 5 mA, input frequency max. 1 Mhz
- 4x Optocoupler outputs, output current max. 20 mA, output frequency max. 1 Mhz

Analog interface (X3)
- 2x ADC channels
- Input voltage range 0-5 V, 0-10 V, ±5 V, ±10 V, separately adjustable for each channel via DIP switch
- Resolution 16 bits
- Offset error max. ±3 mV
- Gain error max. ±5 mV
- Conversion rate max. 150 kHz per channel

5. Installation of IF2008/PCIe

For installing the IF2008/PCIe please proceed as follows:

➡ Switch off your computer as well as all peripheral devices. Unplug the power cords.

➡ Open the housing of your computer. For further details please find the instruction in your computer manual.

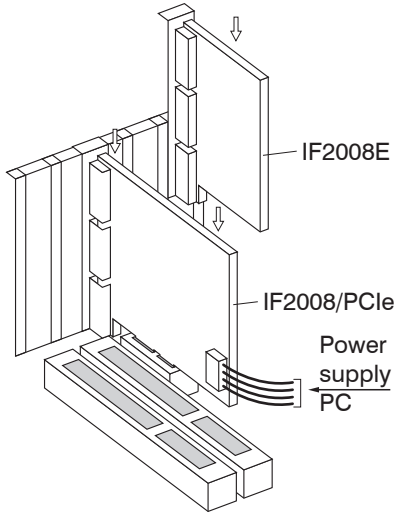
➡ Find a PCI extension slot for the IF2008/PCIe card which is not assigned. Remove the cover of the slot, keep hold of the card on the top edge while carefully pushing it into the slot. The card must be fastened to the mounting using bolts.

i IF2008/PCIe requires on X7 an external supply voltage through PC!

➡ Connect X7 of the IF2008/PCIe with the power supply of the PC. Therewith you support the necessary power supply of the DC-/DC converter.

➡ The IF2008E has to be fastened to a mounting which is not assigned using bolts. Interconnect the interface cards IF2008/PCIe and IF2008E. Connect the plug connectors of the same numbering using the cables which are included in delivery, that means X4 with X4, X5 with X5, X6 with X6.

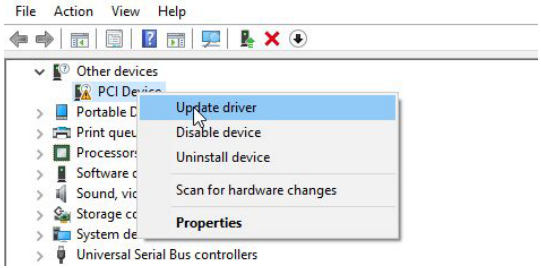
➡ Close the housing of your computer and switch on the computer as well as the peripheral devices.



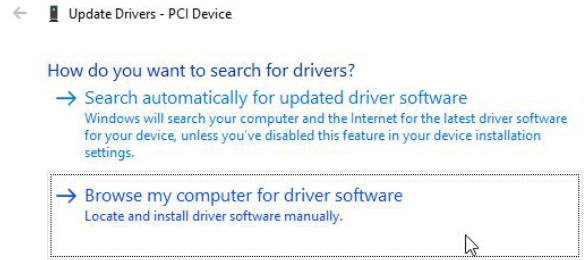
6. Installation of Devices Driver, Windows 10

The installation of a driver may be regulated by your IT department. Install drivers together with your IT department or have a time-limited admin right set up on your PC.

The following notes describe the installation of the driver via the device manager.

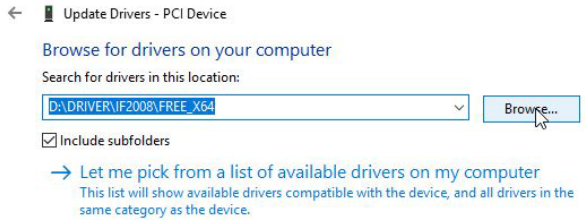


➡ Start the device manager and click the `Update driver` entry.



➡ Choose `Browse my computer for driver software`.

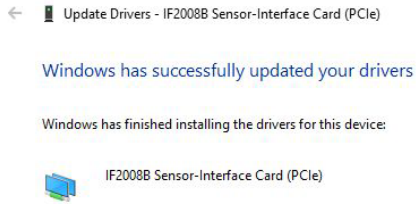
➡ Copy the driver file into the path to MEDAQLib <...Driver/IF2008>.



➡ Click the `Browse` button and enter the path to the driver file. Check the `Include subfolders` box.

➡ In the following screen, set the check mark for `Trust software from ...` and click the `Install` button.

The operating system reports the successful installation of the driver, the device manager lists the interface card.



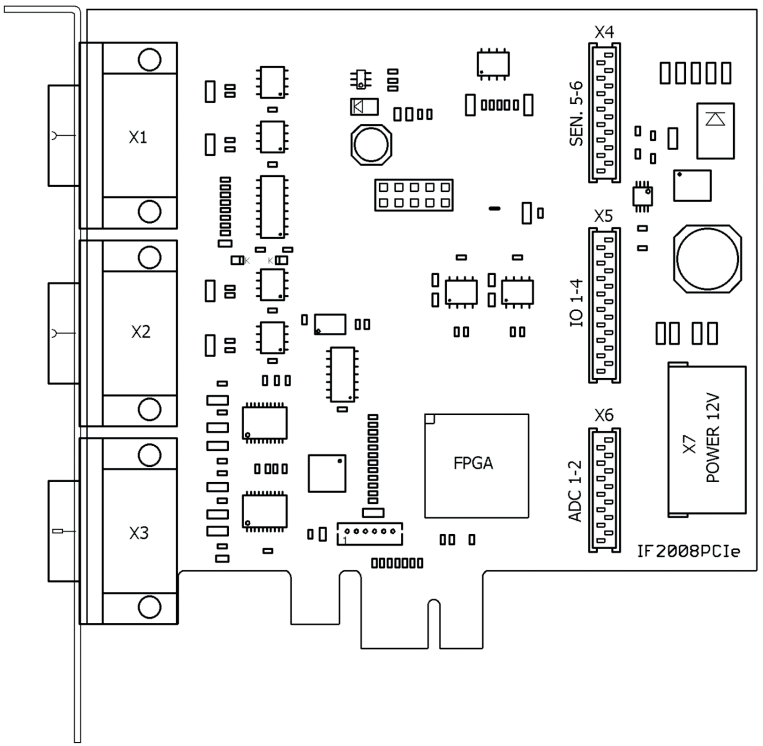
7. Hardware

7.1 View of IF2008/PCIe Basis Board

X1 = Sensor connection 1 and 2

X2 = Sensor connection 3 and 4

X3 = Encoder connection 1 and 2



X4 ... X6 = Connector for IF2008E connection

X7 = Connection 12 V power

Fig. 1: View of board IF2008/PCIe Basis Board

7.2 View of IF2008E Expansion Board

X1 = Sensor connection 5 and 6

X2 = Connection for IO signals

X3 = Connection for A/D converter

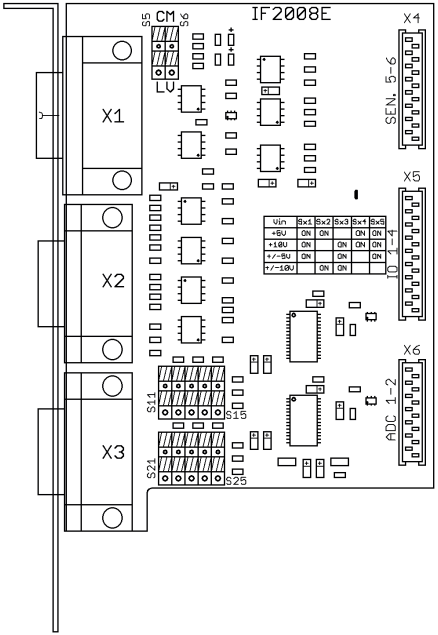


Fig. 2: View of board IF2008E expansion board

X4 ... X6 = Connection for IF2008/PCIe connection

S5 and S6 = Switch for positive trigger level

S11 ... S15 = Switch for ADC level 1

S21 ... S25 = Switch for ADC level 2

8. Pin Assignments and Jumper Settings

8.1 Sensor Interface

IF2008/PCIe X1 and X2, IF2008E X1

Pin	Signal
1	Sensor 1 TxD-
2	Sensor 1 TxD+
3	Sensor 1 RxD-
4	Sensor 1 RxD+
5	Power supply 0 V
6	Sensor 1 TRG+
7	Sensor 1 TRG-
8	Sensor 2 TRG+
9	Sensor 2 TRG-
10	Power supply +24 V
11	Sensor 2 TxD-
12	Sensor 2 TxD+
13	Sensor 2 RxD-
14	Sensor 2 RxD+
15	GND

Fig. 3: Pin assignment for sensor interface

8.2 Encoder Interface

IF2008/PCIe X3

Pin	Function
1	Encoder 1 Track A+
2	Encoder 1 Track A-
3	Encoder 2 Track A+
4	Encoder 2 Track A-
5	VCC (+5 V)
6	Encoder 1 Track B+
7	Encoder 1 Track B-
8	Encoder 2 Track B+
9	Encoder 2 Track B-
10	GND
11	Encoder 1 Track R+
12	Encoder 1 Track R-
13	Encoder 2 Track R+
14	Encoder 2 Track R-
15	GND

Fig. 4: Pin assignment for encoder interface

i The pin assignment is not compatible with IF2004B!

8.3 Sensor Power (IF2008/PCIe X7)

Pin	Function
1	+12 V
2	GND
3	GND
4	n.c.

Fig. 5: Pin assigment of sensor power

8.4 IO Interface (IF2008E X2)

Pin	Function
1	OUT 1
2	OUT 2
3	OUT 3
4	OUT 4
5	GND
6	IN 1
7	IN 2
8	IN 3
9	IN 4

Fig. 6: Pin assignment IO interface

8.5 Analog Interface (IF2008E X3)

Pin	Function
1	Input signal 1
2	Analog GND
3	Input signal 2
4	Analog GND
5	n.c.
6	n.c.
7	n.c.
8	n.c.
9	n.c.

Fig. 7: Pin assignment analog interface

8.6 Jumper/Switch Setting for Trigger Level

By means of the switches S5 and S6 (IF2008E) the positive trigger level for the sensor channels 5 and 6 (IF2008E) can be selected. The negative output always has LVDS level.

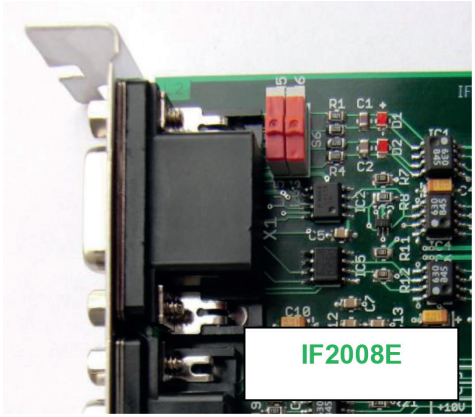


Fig. 8: Switch settings trigger level IF2008A

Switch	Setting	Trigger output +
S5 to S6	LVn	LVDS level for sensor n TRG+
	CMn	3.3 V CMOS level for sensor n TRG+

Fig. 9: Switch settings trigger level

8.7 Switch Setting for ADC Level

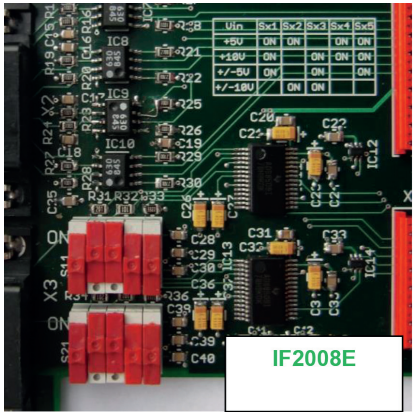


Fig. 10: Switch settings ADC level for ±10 V

VIN	Sx1	Sx2	Sx3	Sx4	Sx5
0-5 V	ON	ON		ON	ON
0-10 V	ON		ON	ON	ON
±5 V	ON		ON		ON
±10 V	OFF	ON	ON		

Fig. 11: Switch settings ADC level

9. Address assignment

9.1 PCI Interface

Interface: PCI-Express x1 interface

Access: Memory space 40 Hex addresses

Base address: Automatically assigned by operating system

Adr.	Byte 3	Byte 2	Byte 1	Byte 0	Value (Hex)
00h	Device ID		Vendor ID		1910 1204
18h	Base Address Local Memory Space				xxxx xxxx
2C	Subsystem ID		Subsystem Vendor ID		2008 1204

Fig. 12: Header configuration

9.2 Local Address Assignment

Base addr. +	Write access	Read access
00h	Transmit register	FIFO data
02h	Set- / Reset- / Latch register	FIFO volume
04h	FIFO enable register	FIFO enable register
06h	Interrupt enable register	Interrupt status register
08h	Sensor 1 baud rate	Reserved
0Ah	Sensor 2 baud rate	Reserved
0Ch	Sensor 3 baud rate	Reserved
0Eh	Sensor 4 baud rate	Reserved
10h	Sensor 5 baud rate	Reserved
12h	Sensor 6 baud rate	Reserved
14h	Counter control register 1	Counter control register 1
16h	Counter control register 2	Counter control register 2
18h	Counter 1 preload LSW	Counter 1 LSW
1Ah	Counter 1 preload MSW	Counter value 1 MSW
1Ch	Counter 2 preload LSW	Counter 2 LSW
1Eh	Counter 2 preload MSW	Counter value 2 MSW
20h	Timer 1 frequency	ADC 1
22h	Timer 1 pulse width	ADC 2
24h	Timer 2 frequency	Status, FPGA- / hardware version
26h	Timer 2 pulse width	Input and status power switch
28h	Timer 3 frequency	Reserved
2Ah	Timer 3 pulse width	Reserved

Base addr. +	Write access	Read access
2Ch	Timer clock splitter	Timer clock splitter
2Eh	Output register	Output register
30h	Mode opto- and TxD outputs	Mode opto- and TxD outputs
32h	Trigger Outputs Mode	Mode trigger outputs, latch source and sensor power switch
34h	ADC control register	ADC-Kontrollregister
36h	Parity enable register	Parity error

Fig. 13: Local address assignment

10. Register Description

10.1 Transmit Register

Base addr. + 00h (write access)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			S6	S5	S4	S3	S2	S1	D7	D6	D5	D4	D3	D2	D1	D0
	Selection sensor channel								Data bits							

Fig. 14: Transmit register

Bit 0 to 7 Include the data for the transmit register
Bit 8 to 15 Select the sensor channel

Bit 8 = 1 > Data are output on the sensor channel S1
Bit 9 = 1 > Data are output on the sensor channel S2

Bit 13 = 1 > Data are output on the sensor channel S6
Bit 14 ... 15 > free

Immediately on the write access to the address „0“, the data with the bit 8 to 13 selected sensor channel are transmitted. The baud rate for the transmit register is automatically adapted to the selected sensor channel. In case that the data output is effected on more channels, the baud rate of the best channel is used.

10.2 Fifo Data

Base addr. + 00h (read access)

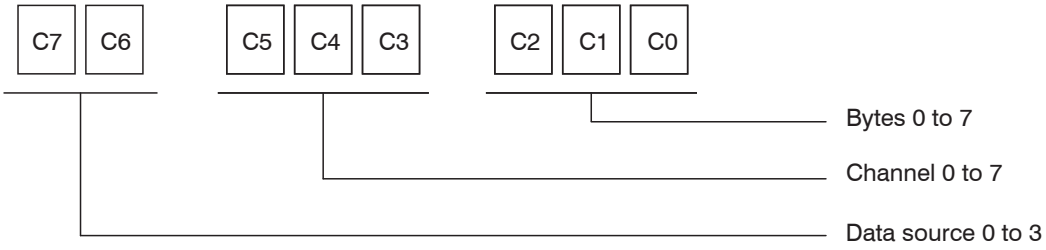
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
	Code bits								Data bits							

Fig. 15: FIFO data memory

Bit 0 to 7 Include the data buffered

Bit 7 to 15 Mark the data code

Code bits



C7	C6	Daten source
0	0	Sensor
0	1	Encoder
1	0	Switching input (IN 1 ... 4 > channel 0, RxD 1 ... 6 > channel 1)
1	1	ADC

Fig. 16: FIFO data memory - data sources

10.3 Set- / Reset- / Latch Register

Base addr.. + 02h (write access)

Bit	Function
0	Delete counter 1
1	Load counter 1
2	Latch counter 1
3	Reference counter 1
4	Delete counter 2
5	Load counter 2
6	Latch counter 2
7	Reference counter 2
8	Start ADC1 conversion
9	Start ADC2 conversion
10	Delete FIFO
11 to 15	Reserved

Fig. 17: Set- / Reset- / Latch register

i By means of the bits 0 to 2 and 4 to 6, the counters can be either deleted or loaded independently of the counter control register by the software, (addr. 14h and addr. 16h). Furthermore, the counter reading can be transferred into the latch register.
If a counter latch or load function, which should only operate in connection with a reference marker signal is settled by the counter control register (addr. 14h and addr. 16h); this is subject to approval by setting bit 3 or bit 7. On setting bit 3 or bit 7 the status bits 0 and 1 or 2 and 3 are reset.
All bits only need to be set, resetting them is not necessary.
After power interruption, all bits are set to “0”.

10.4 FIFO Volume

Base addr. + 02h (read access)

Bit	Function
0 to 14	FIFO data volume (0 to 32767)
15	permanently 0

Fig. 18: FIFO volume

The dataset is transferred automatically into the FIFO data memory on receipt. By means of a report of the FIFO volume the FIFO data amount can be calculated. The order and speed regarding buffering the data received, is similar to the data stream of the receiving register. In case that the FIFO is not readout quickly enough, it offers the latest 32768 data sets.

10.5 FIFO Enable Register

Base addr. + 04h (read and write access)

Bit	Function
0	0 = FIFO for sensor channel 1 disabled 1 = FIFO for sensor channel 1 enabled
1	0 = FIFO for sensor channel 2 disabled 1 = FIFO for sensor channel 2 enabled
2	0 = FIFO for sensor channel 3 disabled 1 = FIFO for sensor channel 3 enabled
3	0 = FIFO for sensor channel 4 disabled 1 = FIFO for sensor channel 4 enabled
4	0 = FIFO for sensor channel 5 disabled 1 = FIFO for sensor channel 5 enabled
5	0 = FIFO for sensor channel 6 disabled 1 = FIFO for sensor channel 6 enabled
6	0 = FIFO for encoder channel 1 disabled 1 = FIFO for encoder channel 1 enabled
7	0 = FIFO for encoder channel 2 disabled 1 = FIFO for encoder channel 2 enabled
8	0 = FIFO for state of external inputs IN 1..4 disabled 1 = FIFO for state of external inputs IN 1..4 enabled
9	0 = FIFO for state of RxD inputs (sensor 1..6) disabled 1 = FIFO for state of RxD inputs (sensor 1..6) enabled
10	0 = FIFO for ADC 1 disabled 1 = FIFO for ADC 1 enabled
11	0 = FIFO for ADC 2 disabled 1 = FIFO for ADC 2 enabled
12	0 = FIFO is disabled for sensor 1 and 2 if ext. input IN 1 is active 1 = IN 1 does not affect FIFO
13	0 = FIFO is disabled for sensor 3 and 6 if ext. input IN 2 is active 1 = IN 2 does not affect FIFO
14	0 = FIFO is disabled for encoder 1 and 2 if ext. input IN 3 is active 1 = IN 3 does not affect FIFO
15	0 = FIFO is disabled for ADC 1/2; IN 1..4; RxD 1..6 if ext. input IN 4 is active 1 = IN 4 does not affect FIFO

Fig. 19: FIFO enable register

10.6 Interrupt Enable Register

Base addr. + 06h (write access)

Bit	Function
0	1 = Enable interrupt requirements if FIFO is filled with more than 50 %
1	1 = Enable interrupt requirements if FIFO is filled with more than 75 %
2	1 = Enable interrupt requirements on overflow Timer 1
3	1 = Enable interrupt requirements on overflow Timer 2
4	1 = Enable interrupt requirements on overflow Timer 3
5	1 = Enable interrupt requirements if external input IN 1 is activated
6	1 = Enable interrupt requirements if external input IN 2 is activated
7	1 = Enable interrupt requirements if external input IN 3 is activated
8	1 = Enable interrupt requirements if external input IN 4 is activated
9 - 15	Reserved

Fig. 20: Interrupt enable register

i The interrupt generation is controlled by a trigger flange, i.e., an interrupt requirement is only effected if the corresponding bit is set in the interrupt enable register. Furthermore, the appropriate source has to change from the inactive into the active state. Several bits can be set at the same time.

10.7 Interrupt-Status-Register

Base addr. + 06h (read access)

Bit	Function
0	1 = Interrupt requirement if FIFO level exceeds 50 %
1	1 = Interrupt requirement if FIFO level exceeds 75 %
2	1 = Interrupt requirement on overflow Timer 1
3	1 = Interrupt requirement on overflow Timer 2
4	1 = Interrupt requirement on overflow Timer 3
5	1 = Interrupt requirement if external input IN 1 is activated
6	1 = Interrupt requirement if external input IN 2 is activated
7	1 = Interrupt requirement if external input IN 3 is activated
8	1 = Interrupt requirement if external input IN 4 is activated
9 - 15	Reserved

Fig. 21: Interrupt status register

i The interrupt state register informs by which source(s) the interrupt requirements have been generated. One interrupt requirement can be effected by using more than one source at the same time. In case that no state bit is set, the interrupt requirement was not generated by the IF2008A but by another hardware.

10.8 Sensor Baud Rate

Base addr.	Sensor channel	Value	Access
+ 08h	1	1 to 65,535	only write access
+ 0Ah	2	1 to 65,535	only write access
+ 0Ch	3	1 to 65,535	only write access
+ 0Eh	4	1 to 65,535	only write access
+ 10h	5	1 to 65,535	only write access
+ 12h	6	1 to 65,535	only write access

Fig. 22: Base addresses for sensor baud rates

Value = (48 MHz / baud rate) - 1

Example:

Desired baud rate = 691.2 kBaud

Value = (48 MHz / 691,200) - 1) = 68,44

The input value must be a whole number, i.e., the result must still be rounded:

> Value = 68

10.9 Counter Control Register

Base addr.	Counter channel	Bit	Access
+ 14h	1	0 to 15	Read and write access
+ 16h	2	0 to 15	Read and write access

Fig. 23: Base addresses for counter control register

The tables below are the same for both counter channels!

Overview of functions:

Bit	Function
0 to 3	Interpolation (see table 21: Encoder interpolation)
4	Counting direction (see table 22: Encoder counter direction)
5 to 7	Counter Mode (see table 23: Counter mode)
8 to 11	Latch source (see table 24: Counter latch source)
12 to 15	Reserved

Fig. 24: Functional overview for counter control register

Interpolation

Bit 3	Bit 2	Bit 1	Bit 0	Interpolation
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	8
0	1	1	1	10
1	0	0	0	12
1	0	0	1	16
1	0	1	0	20
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Interpolation**
1	0	1	1	24
1	1	0	0	32
1	1	0	1	40
1	1	1	0	48
1	1	1	1	64

Fig. 25: Encoder interpolation

i For encoders with 1-Vss signals all interpolations are suitable.
For encoders with TTL-signals the following interpolations are suitable: 1, 2 or 4 times.

Counting direction

Bit 4	Counting direction
0	normal
1	inversed

Fig. 26: Encoder interpolation

Counter mode:

Bit 7	Bit 6	Bit 5	Counter mode
0	0	0	No counter load / delete function by encoder reference marker
0	0	1	Counter is loaded with the next encoder reference marker provided that the state bit 0 or state bit 2 “0” is settled.
0	1	0	Counter is loaded including all encoder reference markers and load register content. State bit 0 to 3 have no effect.
0	1	1	Counter is deleted including all encoder reference markers and additionally loaded with the content of the load register if the counter has reached -1. This function offers the possibility to limit the counter. During this process the counter load register has to be preallocated with the number of increments limited -1.
1	0	0	Counter without phase discriminator (event counter)
			Bit 4 / **Function**
			0 / Track A = counter direction signal
			0 / Track B = counter clock signal
			1 / Track A = counter clock signal
			1 / Track B = counter direction signal
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Fig. 27: Counter mode

Latch source:

Bit 11	Bit 10	Bit 9	Bit 8	Latch source
0	0	0	0	Hardware latch disabled
0	0	0	1	Timer 1
0	0	1	0	Timer 2
0	0	1	1	Timer 3
0	1	0	0	Sensor channel 1
0	1	0	1	Sensor channel 2
0	1	1	0	Sensor channel 3
0	1	1	1	Sensor channel 4
1	0	0	0	Sensor channel 5
Bit 11	**Bit 10**	**Bit 9**	**Bit 8**	**Latch source**
1	0	0	1	Sensor channel 6
1	0	1	0	IN 1 (only with IF2008E expansion board)
1	0	1	1	IN 2 (only with IF2008E expansion board)
1	1	0	0	IN 3 (only with IF2008E expansion board)
1	1	0	1	IN 4 (only with IF2008E expansion board)
1	1	1	0	2nd reference mark
1	1	1	1	all reference marks

Fig. 28: Counter latch source

10.10 Counter Preload

Base addr.	Counter channel	Value	Access
+ 18h	1 LSW	0 to 65.535	only write access
+ 1Ah	1 MSW	0 to 65.535	only write access
+ 1Ch	2 LSW	0 to 65.535	only write access
+ 1Eh	2 MSW	0 to 65.535	only write access

Fig. 29: Base addresses for counter preload

10.11 Counter Value

Base addr.	Counter channel	Value	Access
+ 18h	1 LSW	0 to 65.535	only read access
+ 1Ah	1 MSW	0 to 65.535	only read access
+ 1Ch	2 LSW	0 to 65.535	only read access
+ 1Eh	2 MSW	0 to 65.535	only read access

Fig. 30: Base addresses for counter value

10.12 Timer

Base addr.	Counter channel	Value	Access
+ 20h	1 frequency	0 to 65,535	only write access
+ 22h	1 pulse width	0 to 65,535	only write access
+ 24h	2 frequency	0 to 65,535	only write access
+ 26h	2 pulse width	0 to 65,535	only write access
+ 28h	3 frequency	0 to 65,535	only write access
+ 2Ah	3 pulse width	0 to 65,535	only write access
+ 2Ch	Clock splitter	Read and write access	

Fig. 31: Base addresses for timer

Value (F) = (F_{Clock} / F_{OUT}) - 1

Value (PW) = (PW_{OUT} / T_{Clock})

Example:

Desired frequency F_{OUT} = 10 kHz

Desired pulse width PW_{OUT} = 25 µs

Clock splitter = 0 > F_{Clock} = 24 MHz, T_{Clock} = 41.667 ns (see the following table for clock splitter)

Value (F) = (24 MHz / 10kHz) - 1 = 2399

Value (PW) = (25 µs / 41.667 ns) = 600

The input values must be whole numbers!

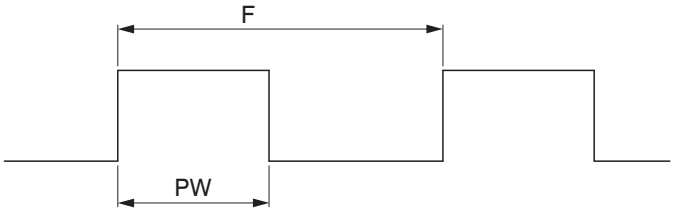


Fig. 32: Timer frequency and pulse width

i The pulse width only affects the “sensor trigger” and “optocoupler” outputs and not the internal synchronization signals. For this, the zero crossing timer is used. To turn off the timer, the frequency must be programmed to be „0“. If pulse width > 0 is programmed when the timer is turned off, output is permanently set to High. However, if the pulse width is also programmed to be „0“, output is permanently set to Low.

Clock splitter:

Bit 3	Bit 2	Bit 1	Bit 0	Clock frequency timer 1
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Clock frequency timer 2**
Bit 11	**Bit 10**	**Bit 9**	**Bit 8**	**Clock frequency timer 3**
0	0	0	0	24 MHz
0	0	0	1	24 MHz / 2
0	0	1	0	24 MHz / 4
0	0	1	1	24 MHz / 8
0	1	0	0	24 MHz / 16
0	1	0	1	24 MHz / 32
0	1	1	0	24 MHz / 64
0	1	1	1	24 MHz / 128
1	0	0	0	24 MHz / 256
1	0	0	1	24 MHz / 512
1	0	1	0	24 MHz / 1024
1	0	1	1	24 MHz / 2048
1	1	0	0	24 MHz / 4096
1	1	0	1	24 MHz / 8192
1	1	1	0	24 MHz / 16384
1	1	1	1	24 MHz / 32768

Fig. 33: Timer clock splitter

i Bit 12 to Bit 15 are reserved.

10.13 ADC

Base addr.	ADC channel	Value	Access
+ 20h	1	0 to 65535	only read access
+ 22h	2	0 to 65535	only read access

Fig. 34: Base addresses for ADC

10.14 Status

Base addr. + 24h (only read access)

Bit	Function
0	1 = Encoder 1: 1st reference mark crossed
1	1 = Encoder 1: 2nd reference mark crossed
2	1 = Encoder 2: 1st reference mark crossed
3	1 = Encoder 2: 2nd reference mark crossed
4	0 = Transmitter ready for new data transfer 1 = Transmitter is occupied
5	0 = No extension module with sensor 5 / 6 available 1 = Extension module with sensor 5 / 6 available
6	0 = No extension module for external I/O available 1= Extension module for external I/O available
7	0 = No extension module with ADC available 1 = Extension module with ADC available
8 – 13	FPGA version
14 – 15	Hardware version

Fig. 35: Status

10.15 Input and Sensor Power Switch Status

Base addr. + 26h (only read access)

Bit	Function
0	1 = Ext. input IN 1 active
1	1 = Ext. input IN 2 active
2	1 = Ext. input IN 3 active
3	1 = Ext. input IN 4 active
4	1 = RxD input on the sensor input 1 active
5	1 = RxD input on the sensor input 2 active
6	1 = RxD input on the sensor input 3 active
7	1 = RxD input on the sensor input 4 active
8	1 = RxD input on the sensor input 5 active
9	1 = RxD input on the sensor input 6 active
10	1 = Error sensor power switch
11 – 15	Reserved

Fig. 36: Input and sensor power switch status

10.16 Output Register

Base addr. + 2Eh (read and write access)

Bit	Function	Output signal
0	0 = OUT 1 OFF Optocoupler disabled [1] 1 = OUT 1 ON Optocoupler conductive	Output 1 = High Output 1 = Low
1	0 = OUT 2 OFF Optocoupler disabled [1] 1 = OUT 2 ON Optocoupler conductive	Output 2 = High Output 2 = Low
2	0 = OUT 3 OFF Optocoupler disabled [1] 1 = OUT 3 ON Optocoupler conductive	Output 3 = High Output 3 = Low
3	0 = OUT 4 OFF Optocoupler disabled [1] 1 = OUT 4 ON Optocoupler conductive	Output 4 = High Output 4 = Low

Bit	Function	Output signal	
4	0 = TxD 1 inactive 1 = TxD 1 active	TxD 1+ = High TxD 1+ = Low	TxD 1- = Low TxD 1- = High
5	0 = TxD 2 inactive 1 = TxD 2 active	TxD 2+ = High TxD 2+ = Low	TxD 2- = Low TxD 2- = High
6	0 = TxD 3 inactive 1 = TxD 3 active	TxD 3+ = High TxD 3+ = Low	TxD 3- = Low TxD 3- = High
7	0 = TxD 4 inactive 1 = TxD 4 active	TxD 4+ = High TxD 4+ = Low	TxD 4- = Low TxD 4- = High
8	0 = TxD 5 inactive [1)] 1 = TxD 5 active	TxD 5+ = High TxD 5+ = Low	TxD 5- = Low TxD 5- = High
9	0 = TxD 6 inactive [1)] 1 = TxD 6 active	TxD 6+ = High TxD 6+ = Low	TxD 6- = Low TxD 6- = High
10	0 = TRG 1 inactive 1 = TRG 1 active	TRG 1+ = Low TRG 1+ = High	TRG 1- = High TRG 1- = Low
11	0 = TRG 2 inactive 1 = TRG 2 active	TRG 2+ = Low TRG 2+ = High	TRG 2- = High TRG 2- = Low
12	0 = TRG 3 inactive 1 = TRG 3 active	TRG 3+ = Low TRG 3+ = High	TRG 3- = High TRG 3- = Low
13	0 = TRG 4 inactive 1 = TRG 4 aktiv	TRG 4+ = Low TRG 4+ = High	TRG 4- = High TRG 4- = Low
14	0 = TRG 5 inaktiv [1)] 1 = TRG 5 aktiv	TRG 5+ = Low TRG 5+ = High	TRG 5- = High TRG 5- = Low
15	0 = TRG 6 inaktiv [1)] 1 = TRG 6 aktiv	TRG 6+ = Low TRG 6+ = High	TRG 6- = High TRG 6- = Low

Fig. 37: Output register

i For all outputs, several signal sources are available. Bits listed above are only connected through in case that the appropriate mode is set (see Table 33: Mode Opto- and TxD Outputs on page 39).

1) Possible only with expansion board.

10.17 Mode Opto- and TxD Outputs

Base addr. + 30h (read and write access)

Bit	Function		
0 and 1	**Bit1**	**Bit 0**	**Function**
	0	0	Output 1 switches Bit 0 with addr. 2Eh
	0	1	Output 1 switches pulse width with Timer 1
	1	0	Output 1 switches pulse width with Timer 2
	1	1	Output 1 switches pulse width with Timer 3
2 and 3	**Bit 3**	**Bit 2**	**Function**
	0	0	Output 2 switches Bit 1 with addr. 2Eh
	0	1	Output 2 switches pulse width with Timer 1
	1	0	Output 2 switches pulse width with Timer 2
	1	1	Output 2 switches pulse width with Timer 3
4 and 5	**Bit 5**	**Bit 4**	**Function**
	0	0	Output 3 switches Bit 2 with addr. 2Eh
	0	1	Output 3 switches pulse width with Timer 1
	1	0	Output 3 switches pulse width with Timer 2
	1	1	Output 3 switches pulse width with Timer 3
6 and 7	**Bit 7**	**Bit 6**	**Function**
	0	0	Output 4 switches Bit 3 with addr. 2Eh
	0	1	Output 4 switches pulse width with Timer 1
	1	0	Output 4 switches pulse width with Timer 2
	1	1	Output 4 switches pulse width with Timer 3

Bit	Function
8	0 = TxD 1 switches with transmitter 1 = TxD 1 switches bit 4 with addr. 2Eh
9	0 = TxD 2 switches with transmitter 1 = TxD 2 switches bit 5 with addr. 2Eh
10	0 = TxD 3 switches with transmitter 1 = TxD 3 switches bit 6 with addr. 2Eh
11	0 = TxD 4 switches with transmitter 1 = TxD 4 switches bit 7 with addr. 2Eh
12	0 = TxD 5 switches with transmitter 1 = TxD 5 switches bit 8 with addr. 2Eh
13	0 = TxD 6 switches with transmitter 1 = TxD 6 switches bit 9 with addr. 2Eh
14-15	Reserved

Fig. 38: Mode Opto- and TxD Outputs

The outputs 1 to 4 are only available for the IF2008E expansion board.

10.18 Mode Trigger Outputs, Latch Source and Sensor Power Switch

Base addr. + 32h (read and write access)

Bit	Function		
0 and 1	**Bit1**	**Bit 0**	**Function**
	0	0	Trigger 1 switches Bit 10 with addr. 2Eh
	0	1	Trigger 1 switches pulse width with Timer 1
	1	0	Trigger 1 switches pulse width with Timer 2
	1	1	Trigger 1 switches pulse width with Timer 3
2 and 3	**Bit 3**	**Bit 2**	**Function**
	0	0	Trigger 2 switches Bit 11 with addr. 2Eh
	0	1	Trigger 2 switches pulse width with Timer 1
	1	0	Trigger 2 switches pulse width with Timer 2
	1	1	Trigger 2 switches pulse width with Timer 3
4 and 5	**Bit 5**	**Bit 4**	**Function**
	0	0	Trigger 3 switches Bit 12 with addr. 2Eh
	0	1	Trigger 3 switches pulse width with Timer 1
	1	0	Trigger 3 switches pulse width with Timer 2
	1	1	Trigger 3 switches pulse width with Timer 3
6 and 7	**Bit 7**	**Bit 6**	**Function**
	0	0	Trigger 4 switches Bit 13 with addr. 2Eh
	0	1	Trigger 4 switches pulse width with Timer 1
	1	0	Trigger 4 switches pulse width with Timer 2
	1	1	Trigger 4 switches pulse width with Timer 3

Bit	Function			
8 and 9	**Bit 9**	**Bit 8**	**Function**	
	0	0	Trigger 5 switches Bit 14 with addr. 2Eh	
	0	1	Trigger 5 switches pulse width with Timer 1	
	1	0	Trigger 5 switches pulse width with Timer 2	
	1	1	Trigger 5 switches pulse width with Timer 3	
10 and 11	**Bit 11**	**Bit 10**	**Function**	
	0	0	Trigger 6 switches Bit 15 with addr. 2Eh	
	0	1	Trigger 6 switches pulse width with Timer 1	
	1	0	Trigger 6 switches pulse width with Timer 2	
	1	1	Trigger 6 switches pulse width with Timer 3	
12-14	**Bit 14**	**Bit 13**	**Bit 12**	**Latch source**
	0	0	0	Hardware latch disabled
	0	0	1	Timer 1
	0	1	0	Timer 2
	0	1	1	Timer 3
	1	0	0	Sensor channel 1
	1	0	1	Sensor channel 2
	1	1	0	Sensor channel 3
	1	1	1	Sensor channel 4
15	Bit 15 = 0 Bit 15 = 1	Sensor power ON (default value after Reset) Sensor power OFF		

Fig. 39: Mode trigger outputs, latch source and sensor power switch

Bits 12 to 14 can be used to select a latch source whose trigger event writes the external trigger inputs (IN 1 to 4) and the RxD inputs (sensor 1 to 6) to FIFO.

10.19 ADC Control Register

Bit 3	Bit 2	Bit 1	Bit 0	Conversion source ADC1
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Conversion source ADC2**
0	0	0	0	Hardware conversion disabled
0	0	0	1	Timer 1
0	0	1	0	Timer 2
0	0	1	1	Timer 3
0	1	0	0	Sensor channel 1
0	1	0	1	Sensor channel 2
0	1	1	0	Sensor channel 3
0	1	1	1	Sensor channel 4
1	0	0	0	Sensor channel 5
1	0	0	1	Sensor channel 6
1	0	1	0	IN 1 (only with IF2008E exüpansion board)
1	0	1	1	IN 2 (only with IF2008E exüpansion board)
1	1	0	0	IN 3 (only with IF2008E exüpansion board)
1	1	0	1	IN 4 (only with IF2008E exüpansion board)
1	1	1	0	Reserved
1	1	1	1	Reserved

Fig. 40: ADC control register bits 0-7

Bit	Function
8	0 = ADC1 data output binary 2-complement 1 = ADC1 data output binary unconverted
9	0 = ADC2 data output binary 2-complement 1 = ADC2 data output binary unconverted
10 – 15	Reserved

Fig. 41: ADC controll register bits 8-15

Analog input				Digital output	
0 – 5 V	**0 – 10 V**	**+/-5 V**	**+/-10 V**	**Binary 2-complement**	**Binary unconverted**
+4.99 V	+9.99 V	+4.99 V	+9.99 V	7FFF	FFFF
2,5 V	5 V	0 V	0 V	0000	8000
+2.499 V	+4.999 V	-153 µV	-305 µV	FFFF	7FFF
0 V	0 V	-5 V	-10 V	8000	0000

Fig. 42: ADC converting result

10.20 Parity Enable Register

Base addr. + 36h (write access)

Bit	Function
0	0 = Parity bit for sensor channel 1 disabled 1 = Parity bit for sensor channel 1 enabled (only even parity)
1	0 = Parity bit for sensor channel 2 disabled 1 = Parity bit for sensor channel 2 enabled (only even parity)
2	0 = Parity bit for sensor channel 3 disabled 1 = Parity bit for sensor channel 3 enabled (only even parity)
3	0 = Parity bit for sensor channel 4 disabled 1 = Parity bit for sensor channel 4 enabled (only even parity)
4	0 = Parity bit for sensor channel 5 disabled 1 = Parity bit for sensor channel 5 enabled (only even parity)
5	0 = Parity bit for sensor channel 6 disabled 1 = Parity bit for sensor channel 6 enabled (only even parity)
6-15	Reserved

Fig. 43: Parity enable register

10.21 Parity-Error-Register

Base addr. + 36h (write access)

Bit	Function
0	1 = Parity-Error sensor channel 1
1	1 = Parity-Error sensor channel 2
2	1 = Parity-Error sensor channel 3
3	1 = Parity-Error sensor channel 4
4	1 = Parity-Error sensor channel 5
5	1 = Parity-Error sensor channel 6
6 – 15	reserviert

Fig. 44: Parity error register

11. Wiring Recommendations

11.1 Sensor ILD1420

Pin IF2008/PCIe	Signal IF2008/PCIe	ILD1420		Signal ILD1420
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	4		RxD-
2	Sensor 1 TxD+	3		RxD+
3	Sensor 1 RxD-	6		TxD-
4	Sensor 1 RxD+	5		TxD+
5	Power supply 0 V	12	12	GND
6	Sensor 1 TRG+	9		TeachIn
7	Sensor 1 TRG-	n.c.	n.c.	
8	Sensor 2 TRG+		9	TeachIn
9	Sensor 2 TRG-	n.c.	n.c.	
10	Power supply +24 V	7	7	+UB
11	Sensor 2 TxD-		4	RxD-
12	Sensor 2 TxD+		3	RxD+
13	Sensor 2 RxD-		6	TxD-
14	Sensor 2 RxD+		5	TxD+
15	GND (galvanically separated to GND PC)	12	12	GND

Fig. 45: Table 40: Sensor wiring ILD1420

11.2 Sensor ILD1750

Pin IF2008/PCIe	Signal IF2008/PCIe	ILD1750		Signal ILD1750
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	11		RxD-
2	Sensor 1 TxD+	12		RxD+
3	Sensor 1 RxD-	2		TxD-
4	Sensor 1 RxD+	1		TxD+
5	Power supply 0 V	6	6	GND
6	Sensor 1 TRG+	3		TRG+
7	Sensor 1 TRG-	4		TRG-
8	Sensor 2 TRG+		3	TRG+
9	Sensor 2 TRG-		4	TRG-
10	Power supply +24 V	5	5	+UB
11	Sensor 2 TxD-		11	RxD-
12	Sensor 2 TxD+		12	RxD+
13	Sensor 2 RxD-		2	TxD-
14	Sensor 2 RxD+		1	TxD+
15	GND (galvanically separated to GND PC)	6	6	GND

Fig. 46: Sensor wiring ILD1750

11.3 Sensor ILD2300

Pin IF2008/PCIe	Signal IF2008/PCIe	ILD2300		Signal ILD2300
		Pin sensor 1	Pin sensor 2	
1	Sensor 1 TxD-	8		RxD-
2	Sensor 1 TxD+	7		RxD+
3	Sensor 1 RxD-	10		TxD-
4	Sensor 1 RxD+	9		TxD+
5	Power supply 0 V	2	2	Supply ground
6	Sensor 1 TRG+	5		SyncIn+
7	Sensor 1 TRG-	6		
8	Sensor 2 TRG+		5	SyncIn+
9	Sensor 2 TRG-		6	
10	Power supply +24 V	1	1	+UB
11	Sensor 2 TxD-		8	RxD-
12	Sensor 2 TxD+		7	RxD+
13	Sensor 2 RxD-		10	TxD-
14	Sensor 2 RxD+		9	TxD+
15	GND (galvanically separated to GND PC)	2	2	SyncIn-

Fig. 47: Sensor wiring ILD2300

11.4 Encoder Interface

Pin X3 IF2008/PCIe	Signal IF2008/PCIe	1 Vss or RS422		TTL (single-ended)	
		Signal Encoder 1	Signal Encoder 2	Signal Encoder 1	Signal Encoder 2
1	Encoder 1 track A+	A+		A	
2	Encoder 1 track A-	A-		open	
3	Encoder 2 track A+		A+		A
4	Encoder 2 track A-		A-		open
5	VCC (+5 V)	+UB	+UB	+UB	+UB
6	Encoder 1 track B+	B+		B	
7	Encoder 1 track B-	B-		open	
8	Encoder 2 track B+		B+		B
9	Encoder 2 track B-		B-		open
10	GND	GND	GND	GND	GND
11	Encoder 1 track R+	R+		R	
12	Encoder 1 track R-	R-		open	
13	Encoder 2 track R+		R+		R
14	Encoder 2 track R-		R-		open
15	GND	GND	GND	GND	GND

Fig. 48: Encoder interface

i Plus inputs (A+, B+, R+) may not remain open. For example, if only the clock signal is used, the plus inputs have to be set on GND or VCC.

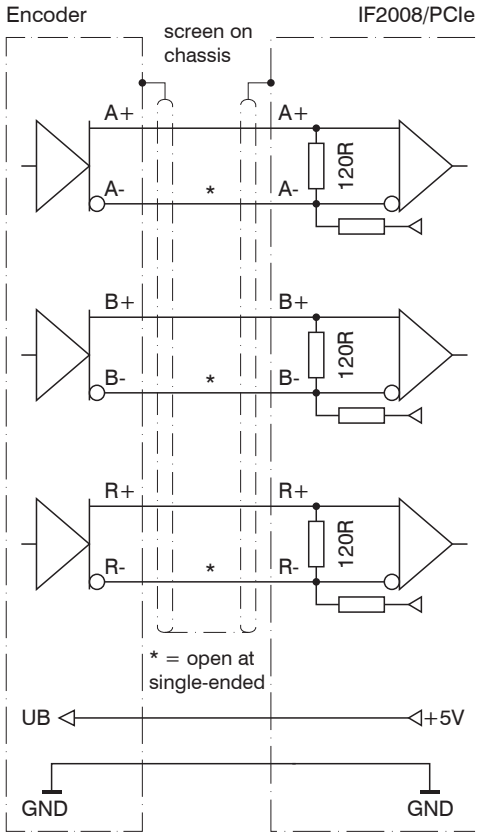


Fig. 49: Block diagram encoder interface

11.5 Optocoupler I/O

Pin IF2008/PCIe	Signal IF2008/PCIe		Pin IF2008/PCIe	Signal IF2008/PCIe
1	OUT 1		6	IN 1
2	OUT 2		7	IN 2
3	OUT 3		8	IN 3
4	OUT 4		9	IN 4
5	GND			

Fig. 50: Optocoupler I/O

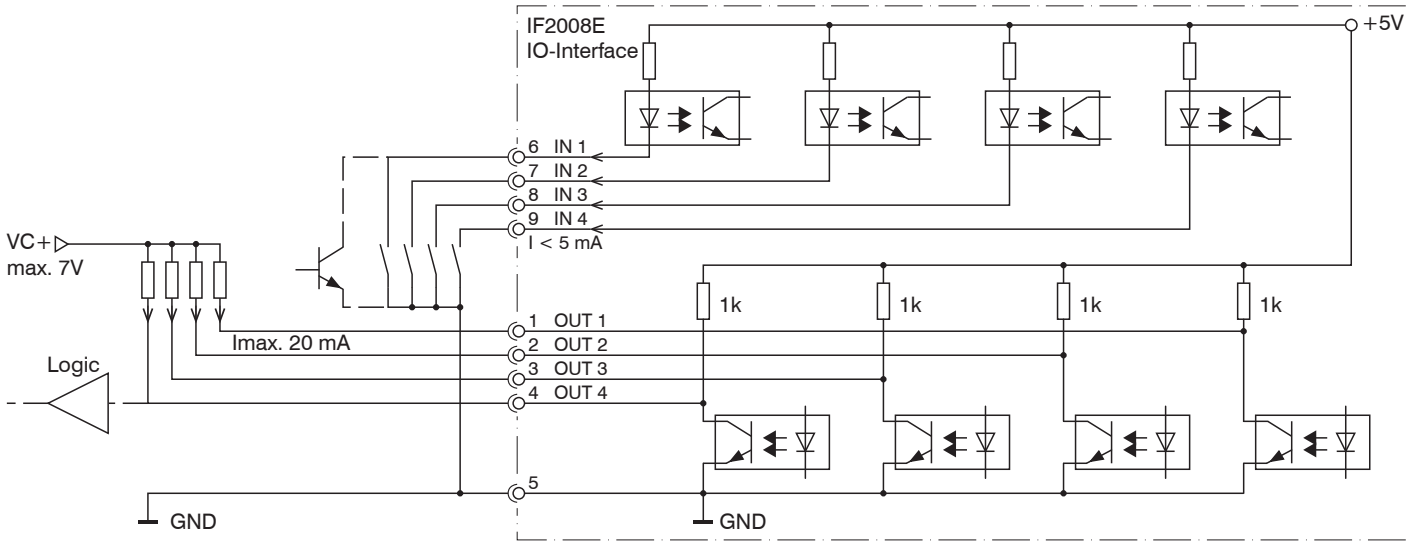


Fig. 51: Block diagram optocoupler I/O

12. Liability for Material Defects

All components of the device have been checked and tested for functionality at the factory. However, if defects occur despite our careful quality control, MICRO-EPSILON or your dealer must be notified immediately.

The liability for material defects is 12 months from delivery. Within this period, defective parts, except for wearing parts, will be repaired or replaced free of charge, if the device is returned to MICRO-EPSILON with shipping costs prepaid. Any damage that is caused by improper handling, the use of force or by repairs or modifications by third parties is not covered by the liability for material defects.
Repairs are carried out exclusively by MICRO-EPSILON.

Further claims can not be made. Claims arising from the purchase contract remain unaffected. In particular, MICRO-EPSILON shall not be liable for any consequential, special, indirect or incidental damage. In the interest of further development, MICRO-EPSILON reserves the right to make design changes without notification.

For translations into other languages, the German version shall prevail.

13. Decommissioning, Disposal

➡ Remove the power supply cable and all output cables from the interface card(s).

Incorrect disposal may cause harm to the environment.

➡ Dispose of the device, its components and accessories, as well as the packaging materials in compliance with the applicable country-specific waste treatment and disposal regulations of the region of use.

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